

REMARKS/ARGUMENTS

Claims 65-77 are pending. In the Office Action mailed July 31, 2007 (designated "Final"), claims 65-72 were rejected under 35 U.S.C. § 101 for non-statutory subject matter; claims 65-77 were rejected under 35 U.S.C. § 112, second paragraph for indefiniteness; claims 65, 66, and 72-77 were rejected under 35 U.S.C. § 102 as anticipated by US Patent Publication 2002/0051394 to Tobita; claims 67-71 were rejected under 35 U.S.C. § 102(b) as anticipated by US Patent No. 4,969,121 to Chan; and claims 67-71 were rejected under 35 U.S.C. § 102(b) as anticipated by US Patent No. 6,075,723 to Naiki. This amendment provides amendments to the claims as described further below, in view of the Section 112 rejections. Accompanying this amendment is a Request for Continued Examination (RCE) for entry of the amendments. No new matter has been added. It is asserted that the claims, as amended, meet the requirements of Section 101 and Section 112, and are patentable over the cited references. Further examination and reconsideration are requested.

Section 101

The wording of claims 65-72 in a strictly conditional manner were stated to be non-statutory as not creating a "useful, concrete and tangible result." Although Applicants contest such a characterization, claim amendments are nevertheless presented in consideration of the Section 112 rejections that, it is asserted, should remove the Section 101 rejection. In particular, claim 65 now recites that a write operation is detected and is performed at a first speed if the write operation is to a first address area and is performed at a second speed if the write operation is not directed to the first address area. A similar change has been made to claim 67. Thus, it is asserted that the claim does not recite only conditional operations and that a useful, concrete, tangible result is ensured.

Section 112

The issues of indefiniteness raised in the Office Action have been reviewed and are addressed by the claim amendments. For example, in claim 65, the address of the write operation has been clarified to recite that it indicates a write operation to the first address. The

write operation speeds have been clarified in claims 65 and 73. The time for the write operations has been clarified in claims 66 and 77. The access mode "corresponding" to a register and address indication have been clarified in claim 67. The cache memory operations have been clarified in claim 68. The address indicating register phrase in claim 71 has been clarified by the amendment to claim 67. The write operations issues in claims 65 and 72 have been corrected by amendment. Claims 69, 70, and 75 have been amended in similar fashion to include the same corrections. It is asserted that claims 65-77 meet the requirements of Section 112.

Section 102 Rejection Over Tobita

The Section 102 rejection over Tobita for claims 65, 66, and 72-77 is traversed with respect to the claims as amended. The Office Action asserted that Tobita recording data words at a fast write speed for high order bits and at a slow write speed for low order bits anticipated the invention. It is asserted that Tobita does not write data to memory at a first write speed if the write operation is indicated to a first address area and write at a second write speed if the write operation is not to the first address area. Rather, Tobita processes a write operation to an address so as to break up the data words to write into two areas. Thus, the write operation to a single address is split up into two write operations, so that high order bits and lower order bits are stored in different locations (see col. 17, paragraph 0240). This operation does not meet the claim language of claims 65, 66, and 72-77, which therefore are not anticipated.

Section 102 Rejection Over Chan

The Section 102 rejection of claims 67-71 as anticipated by Chan is traversed with respect to the claims as amended. The Office Action asserts that Chan shows a fast write and slow write mode that are selected by elements 34, 36 of a logic array and that therefore claims 67-71 are anticipated. The claims as amended, however, recite determining an access mode according to a value in a register, and then performing a write operation in accordance with the access mode, in any one of four modes. In contrast, Chan shows two circuit components 34, 36 (they appear to be FETs) that, in any case, are "EPROM elements" that select slow write, apparently using a high/low signal level (see col. 7, lines 30-34 and lines 62-68, and see Fig. 4). It is asserted that such componentry with high/low signals does not anticipate the

recited register with value that indicates one of four modes. Thus, it is asserted that Chan does not anticipate claims 67-71, as amended.

Section 102 Rejection Over Naiki

The rejection of claims 67-71 over Naiki is traversed with respect to the claims as amended. The Office Action asserted that the long play and short play modes of Naiki anticipate the access modes of the claims. It is noted that Naiki mentions a long play (LP) mode in which there is a reduction in write/erase speed, as well as a short play (SP) mode in which there is no reduction in the write/erase speed. See column 5, lines 28-35. This configuration, however, cannot provide the claimed mode register having a value from which access mode can be determined to be one of four modes. Thus, it is asserted that Naiki does not anticipate any of claims 67-71, as amended.

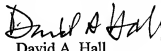
It is asserted that all claims, as amended, meet the requirements of Section 101 and Section 112, and are patentable over the cited references.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 858-350-6100.

Respectfully submitted,


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